line 13, delete "of" and insert -- to --;

line 15, insert -- to be necessary -- after "considered";

line 18, delete "the" and insert -- such an --;

lines 24-25, delete "Japanese Patent Application No. 56-57143 (Japanese laid-open patent application No. 57-172761)" and insert -- U.S. Patent 4,482,985, issued to Itoh, et al. which is incorporated herein by reference --. B2

Page 2, line 8, delete ",";

line 9, delete "and they" and insert -- which --;

line 13, insert -- an -- after "such";

line 17, insert -- terminology -- after "The" and delete "is such that," and insert -- as used herein identifies a test performed --; B3

line 18, delete "," and insert -- during which --;

line 20, delete ",";

line 21, delete "thereby" and delete "which is liable";

line 22, delete "to" (first occurrence) and insert -- for --.

Page 3, line 4, delete "Japanese Patent Application No. 56-168698" and insert -- U.S. Patent 4,482,985 --;

line 7, delete "application" and delete "the" and insert -- that --;

line 17, delete "of Japanese Patent Application" and insert -- disclosed in U.S. Patent 4,482,985 --;

line 18, delete "No. 56-168698".

Page 4, line 23, insert -- prior art voltage regulators and Figures 13B and 14B show -- after "show", delete "13" and insert -- 13(A) to (C), delete "14" and insert -- 14(A) to (C) --and insert --formation of the -- after "the";

line 24, insert -- and characteristics of such practicable forms -- after "forms".

Page 7, line 14, delete "14" and insert -- 23 --;

line 15, delete "Japanese Patent Application No. 56-168698 already filed" and insert -- U.S. Patent 4,482,985 --.

Page 8, line 3, delete "lowers" and insert -- decreases --;

line 17, delete "Japanese Patent Application No. 56-168698" and insert -- U.S. Patent 4,482,985 --.

Page 9, line 9, delete "the";

line 10, delete "well", insert -- if desired -- after "used" and delete "the".

N.E. Page 11, line 18, delete "transistor" and insert -- transistors --, delete "geometry" and insert -- geometries receiving V_{CC} to stress voltage conditions of transistor of small geometries receiving V_L" and delete "and";

line 19, delete "a transistor of small geometry" and delete "Japanese";

line 20, delete "Patent Application No. 56-168698." and insert -- U.S. Patent 4,482,985. Specifically, large geometry devices such as those found in the interface circuit B of Fig. 2 are operated during aging tests at a higher potential than small geometry devices in circuit A at the reduced potential produced by voltage converter 13. --.

N.E. Page 15, line 1, delete "13" and insert -- 13A --, delete "a" and insert -- an -- and delete "practicable".

Page 21, line 5, delete "from" and insert -- between --;

line 9, delete ";" and insert -- : --.

Page 24, line 3, insert -- is expressed -- before "by";

line 8, insert -- can be varied -- before "by";

line 13, delete "any" and insert -- some --.

Page 26, line 17, delete "supposed" and insert -- presumed to be --;

line 21, delete "stuck" and insert -- limited --

.

Page 27, line 24, insert -- it is more of a concern that before "V_G" and delete "is more feared to" and insert -- may --;

line 25, delete "and to" and insert -- which can --.

Page 28, line 1, delete "any" and insert -- some --.

Page 32, line 2, insert -- an -- before "integral" and delete "times" and insert -- multiple --;

line 5, delete "more" and insert -- further --;

line 7, insert -- a -- after "such";

line 8, insert -- The feature of this circuit is that to enhance the driving ability of internal power supply circuit (voltage converter 13) when the load circuit (LCI) operates and to reduce power consumption of internal power supply circuit when the load circuit (LCI) does not operate. Therefore, the operation of this circuit is controlled corresponding to operation states of the load circuit. This internal power supply circuit achieves low power consumption and large driving ability so as to drive a large load circuit quickly. -- after "can be driven.";

lines 11-14, delete "Problematic here is the load driving ability of Q_4 which serves to charge a large capacitance C_D in the load LCI at high speed." and insert -- Problematic here is the characteristic of the load circuit LCI. The load circuit LCI becomes large capacitance CD at one time

and small capacitance at other times. The change of load capacitance is controlled by control signals ϕ_1 and ϕ_2. When the load capacitance is large, the load driving ability of Q4 may be increased so as to charge the load circuit quickly.

line 16, insert -- The boosting node 2 makes driving ability of Q4 larger. -- before "Transistors" and delete "therefor are";

line 17, insert -- are provided for boosting the node 2 -- after "C_1 and C_2";

line 18, insert -- the -- after "to" and insert -- state -- before "of";

line 19, insert -- control signal -- after "the next" also delete "is 'on'" and insert -- is in the "on" state --;

line 20, insert -- the -- after "by";

line 21, insert -- state -- before "of" (first occurrence).

Page 33, line 1, delete "fast" and insert -- rapidly --;

line 2, insert -- control signal -- after "boosted by" and insert -- control signal -- after "When";

line 17, delete "2" and insert -- 3 -- and delete "3" and insert -- 2 --.

Page 36, line 21, delete "whilst" and insert -- while --;

line 24, delete "the" and insert -- an --.